

FIG.2

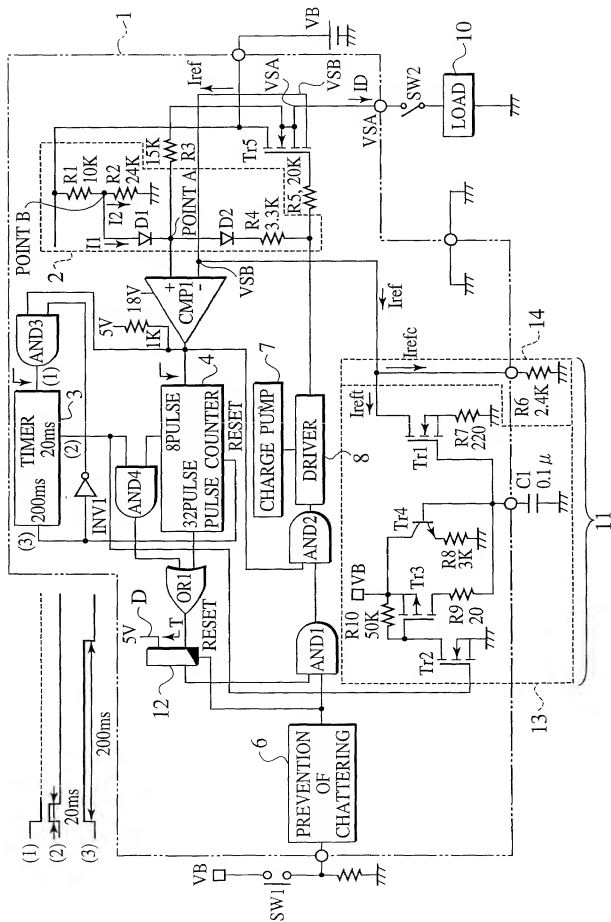


FIG.3

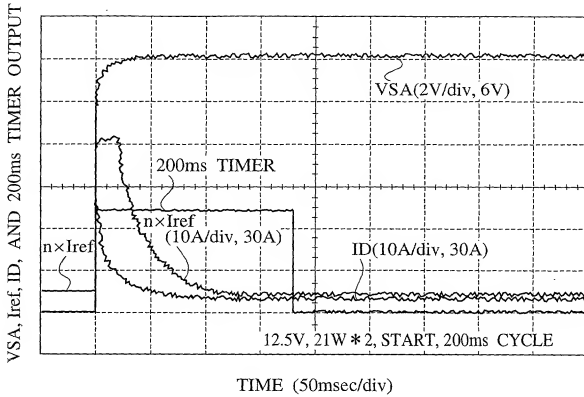


FIG.4

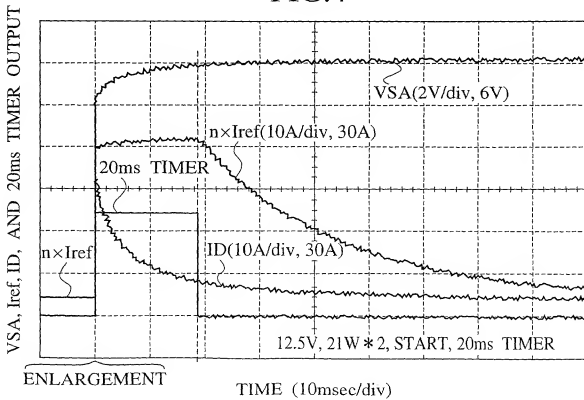


FIG.5

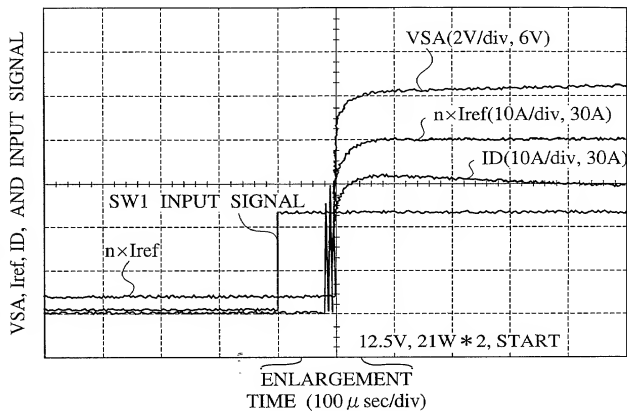
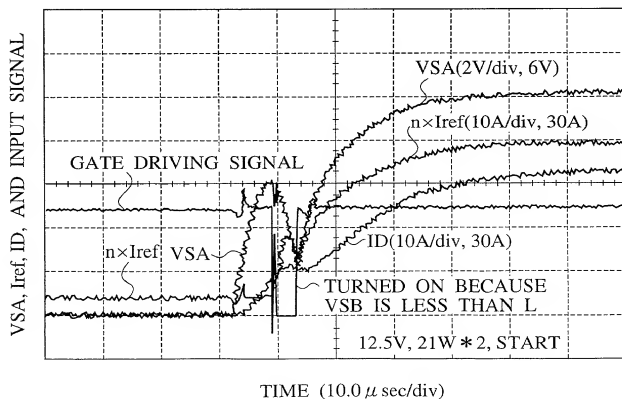
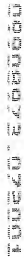


FIG.6



VSA, I_{ref}, ID, AND INPUT SIGNAL

VSA, Iref, ID, AND INPUT SIGNAL

FIG.9

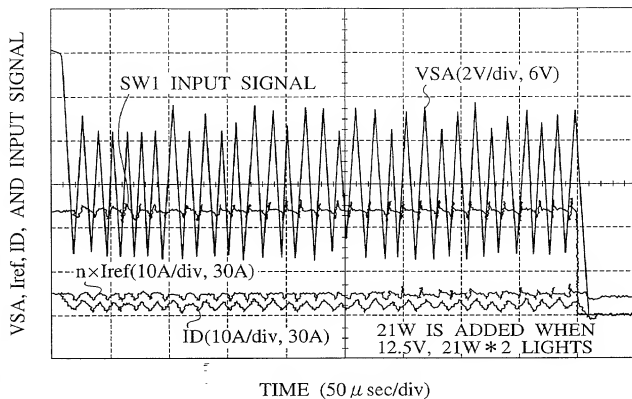


FIG.10

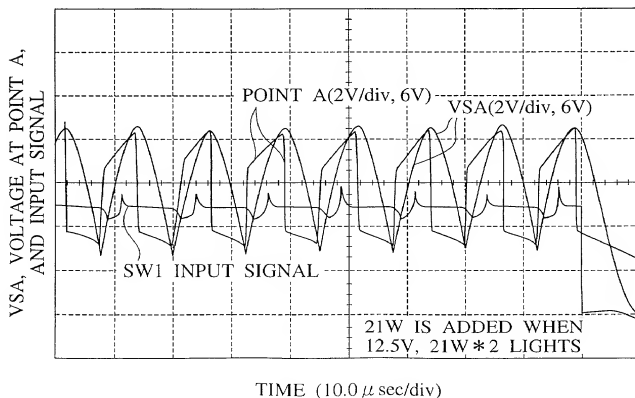


FIG.11

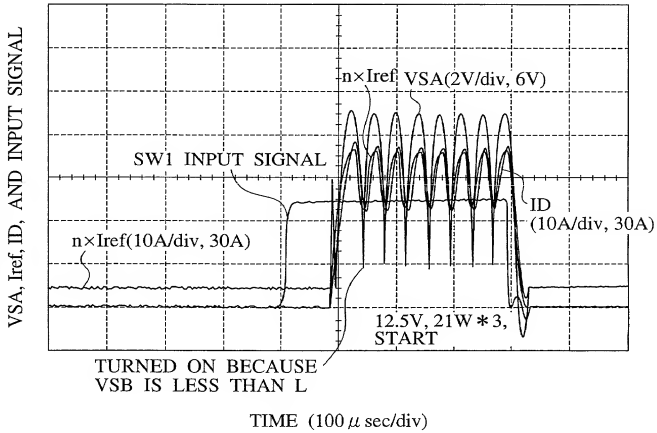


FIG.12

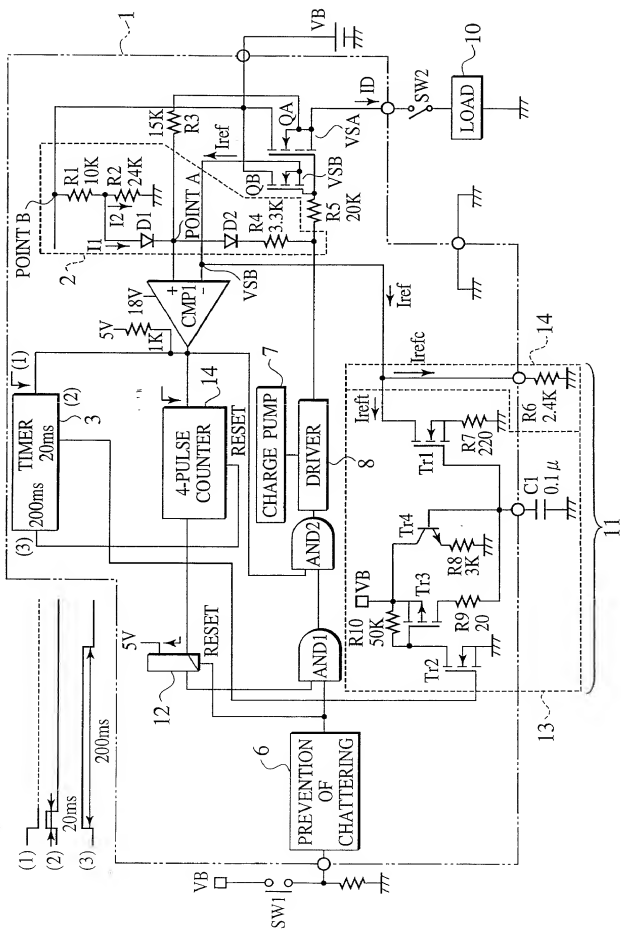
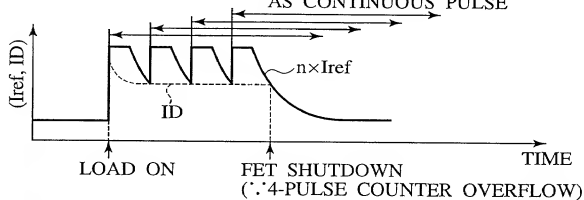
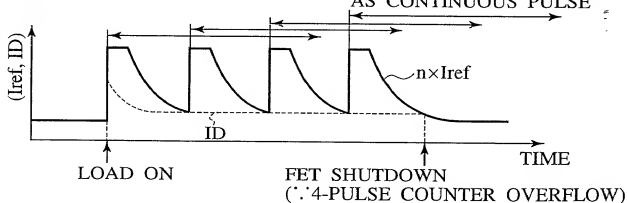


FIG.13

(A) MIDDLE OVERLOAD

THIS PERIOD IS REGARDED
AS CONTINUOUS PULSE

(B) SMALL OVERLOAD

THIS PERIOD IS REGARDED
AS CONTINUOUS PULSE

(C) MULTIPLE LOADS

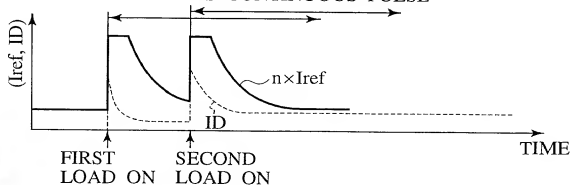
THIS PERIOD IS REGARDED
AS CONTINUOUS PULSE

FIG.14

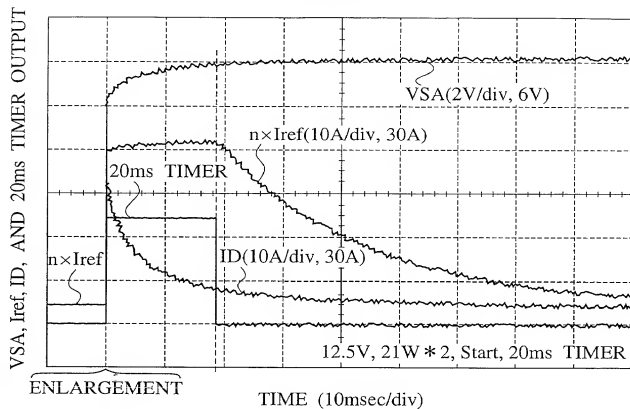
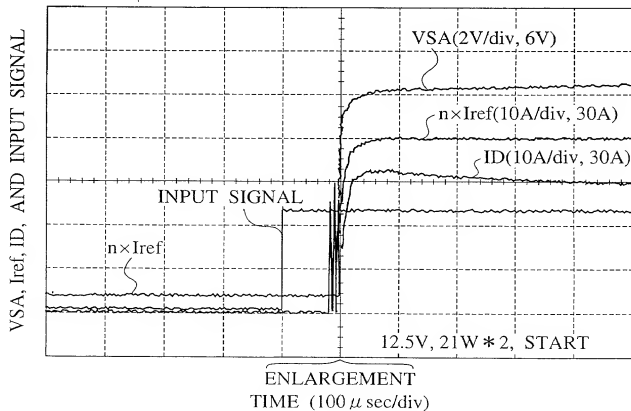


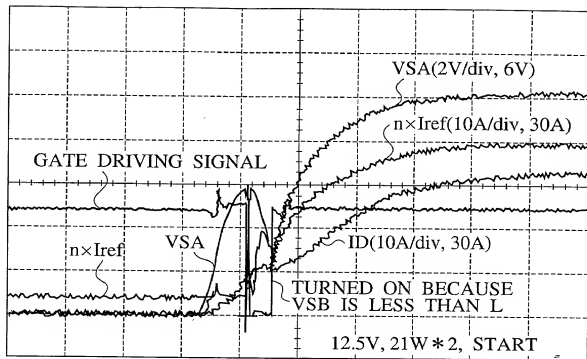
FIG.15



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FIG.16

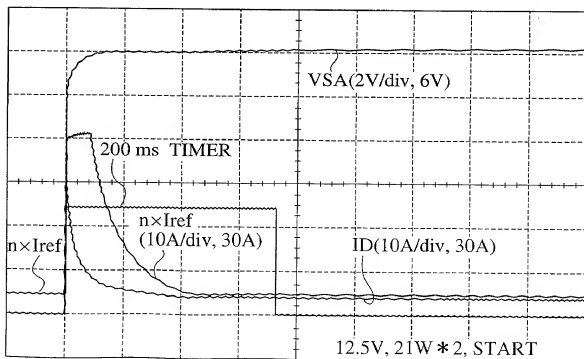
VSA, Iref, ID, AND GATE DRIVING SIGNAL



TIME (10 μ sec/div)

FIG.17

VSA, Iref, ID, 200ms TIMER



TIME (50msec/div)

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FIG.18

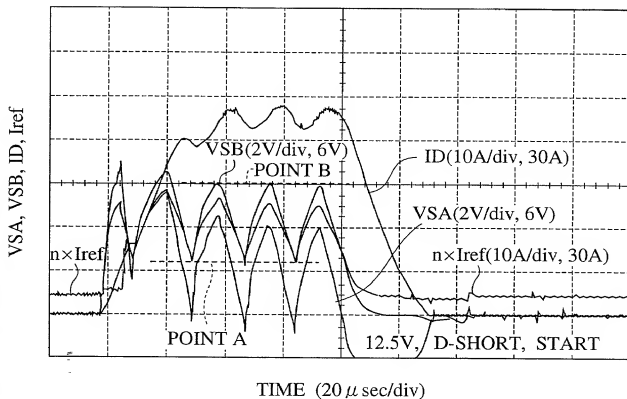


FIG.19

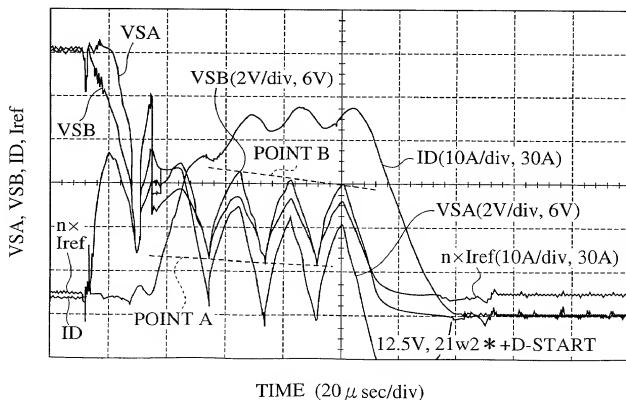
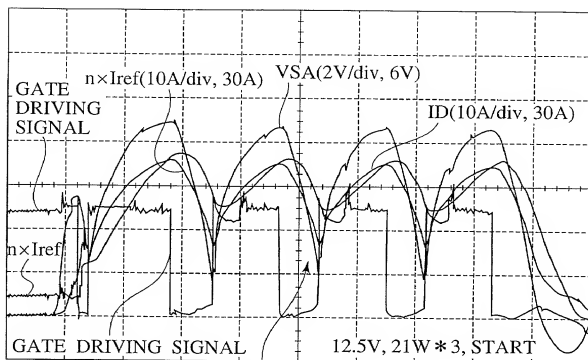


FIG.20

VSA, Iref, ID, AND GATE DRIVING SIGNAL

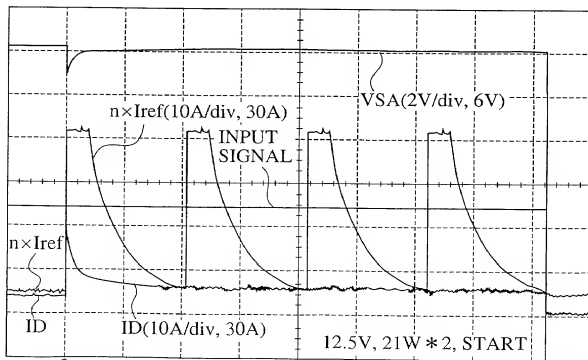


TURNED ON BECAUSE VSB IS
DUMY VOLTAGE LOW OR LESS

TIME (20 μ sec/div)

FIG.21

VSA, Iref, ID, AND INPUT SIGNAL



ENLARGEMENT

TIME (50msec/div)

ENLARGEMENT

FIG.22

VSA, Iref, ID, AND GATE DRIVING SIGNAL

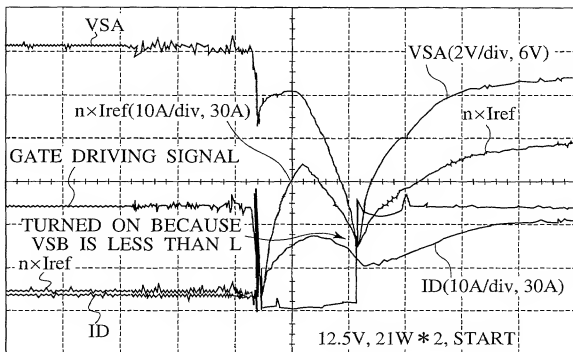
TIME (10 μ sec/div)

FIG.23

VSA, Iref, ID, AND GATE DRIVING SIGNAL

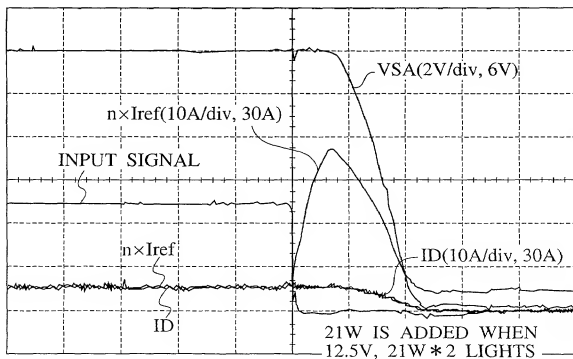
TIME (10 μ sec/div)

FIG.24

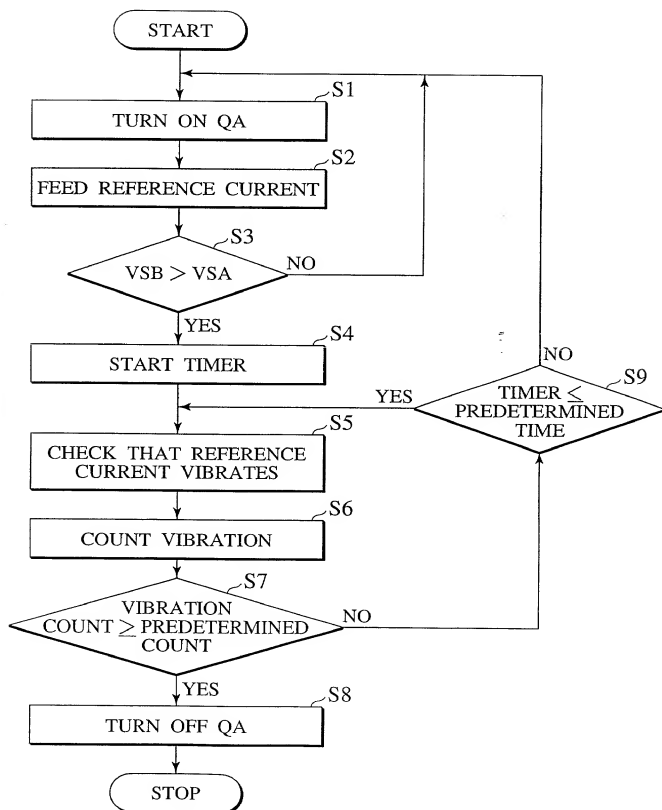


FIG.25

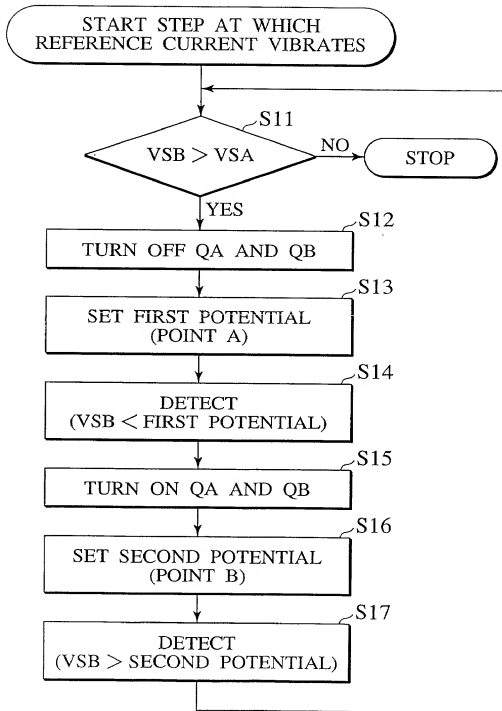


FIG.26

